The ADT7475 controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7475 can drive a fan using either a

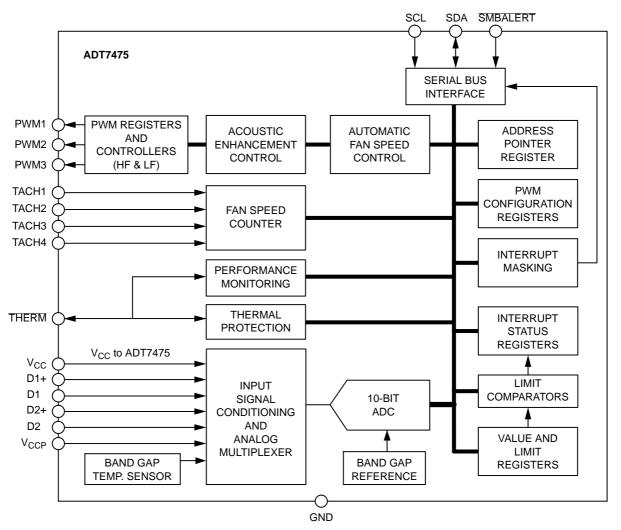


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V _{CC})	3.6	V
Voltage on Any Input or Output Pin	0.3 to +3.6	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA

Maximum Junction Temperature (T_J

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description	
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.	
2	GND	Ground Pin.	
3	V _{CC}	Power Supply. V _{CC} is also monitored through this pin.	
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.	
5	PWM2	PWM2: Digital Output (Open Drain). Requires 10 k Ω typical pullup. Pulse-width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive.	
	SMBALERT	SMBALERT: Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.	
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 1.	
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 2.	
8	PWM3	Digital I/O (Open Drain). Pulse-width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 k Ω typical pullup. Can be configured as a high or low frequency drive.	
9	TACH4 THERM	TACH4: Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 4. THERM: Digital I/O (Open Drain). Alternatively, this pin can be reconfigured as a bidirectional THERM pin that can be used to time and monitor assertions on the THERM input. For example, the pin can be connected to the PROCHOT output of an Intel Pentium 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions.	
	GPIO	GPIO: General-Purpose Open Drain Digital I/O.	
	SMBALERT	SMBALERT: Digital Output (Open Drain). This pin can be reconfigured as an SMBALERT interrupt output to signal out-of-limit conditions.	
10	D2	Cathode Connection to Second Thermal Diode.	
11	D2+	Anode Connection to Second Thermal Diode.	
12	D1	Cathode Connection to First Thermal Diode.	
13	D1+	Anode Connection to First Thermal Diode.	
14	VCCP	Analog Input. Monitors processor core voltage (0 V to 3.0 V).	
15	PWM1	Digital Output (Open Drain). Pulse-width modulated output to control Fan 1 speed. Requires 10 k Ω typical pullup.	
	ХТО	Also functions as the output from the XNOR tree in XNOR test mode.	
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 k Ω typical pullup.	

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = V_{MIN}$ to V_{MAX} , unless otherwise noted.) (Note 1)

Parameter	Conditions	Min	Тур	Max	Unit	
DIGITAL INPUT CURRENT						•
Input High Current, I _{IH}	V _{IN} = V _{CC}		±1		μΑ	
Input Low Current, I _{IL}	V _{IN} = 0 V		±1		μΑ	
Input Capacitance, CIN			5		pF	
SERIAL BUS TIMING (Note 2) (See Fig	jure 2)			•		•
Clock Frequency, f _{SCLK}		10		36 0591	.68 0;31 13.4	9341 i 9.811 56
Glitch Immunity, t _{SW}				50	ns	
Bus Free Time, t _{BUF}		4.7			μS	
SCL Low Time, t _{LOW}		4.7			μS	
SCL High Time, t _{HIGH}		4.0		50	μS	Ĩ
SCL, SDA Rise Time, t _R				1,000	ns	Ī

SCL, SDA Fall Time, t

TYPICAL PERFORMANCE CHARACTERISTICS

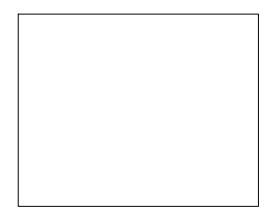


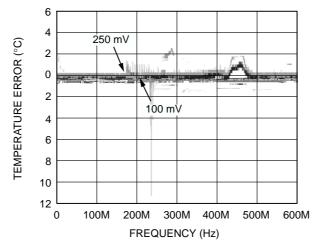
Figure 3. Temperature Error vs. Capacitance Between D+ and D- Figure 4. Remote Temperature Error vs. PCB Resistance

Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency

Figure 7. Normal I_{DD} vs. Power Supply

Figure 8. Internal Temperature Error vs. Power Supply Noise

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)





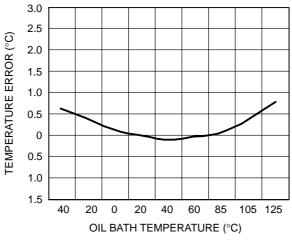
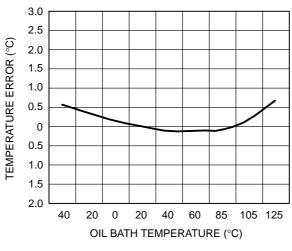
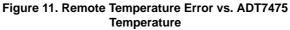


Figure 10. Internal Temperature Error vs. ADT7475 Temperature





Product Description

The ADT7475 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7475 are performed over the serial bus. In addition, a pin can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Quick Comparison Between ADT7473 and ADT7475

- The ADT7473 supports advanced dynamic T_{MIN} features while the ADT7475 does not.
- Acoustic smoothing is improved on the ADT7475.
- THERM can be selected as an output only on the ADT7475.
- The ADT7475 has two additional configuration registers.
- The ADT7475 has other minor register changes.

The ADT7475 is similar to the ADT7473 in that it is

the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7475, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed, and then data can be written to that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 13. The device address is sent over the bus, and then R/\overline{W} is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to write to, which is

stored in the address pointer register. The second data byte is the data to write to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7475 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7475 as before, but only the data byte containing the register address is sent, because no data is written to the register see Figure 14.

A read operation is then performed consisting of the serial bus address; the R/\overline{W} bit set to 1, followed by the data byte read from the data register see Figure 15.

2. If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register see Figure 15.

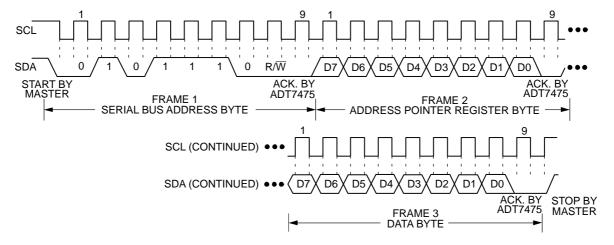
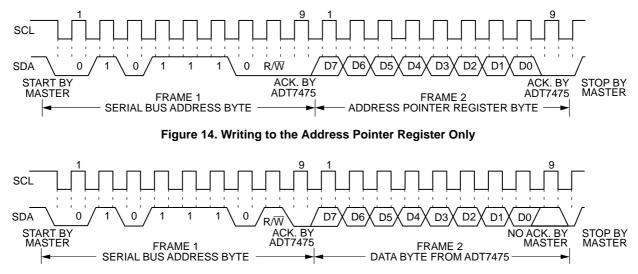
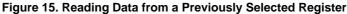


Figure 13. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register





It is possible to read a data byte from a data register without first writing to the address pointer register if the

master. If a device's <u>SMBALERT</u> line goes low, the following events occur:

- 1. **SMBALERT** is pulled low.
- 2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This general call address must not be used as a specific device address.
- 3. The device whose SMBALERT output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
- 4. If more than one device's <u>SMBALERT</u> output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
- 5. Once the ADT7475 has responded to the alert response address, the master must read the status registers, and the <u>SMBALERT</u> is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7475 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7475 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 5. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description	
<6> TODIS	0: SMBus Timeout Enabled (Default)	
	1: SMBus Timeout Disabled	

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7475 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7475 is powered down and powered up again. For more information on which registers are locked, see the Register Tables section.

Voltage Measurement Input

The ADT7475 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings have been made internally, and the results averaged, before being placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μ s), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7475 into single-channel ADC conversion mode. In this mode, the ADT7475 can be made to read a single voltage channel only. If the internal ADT7475 clock is used, the selected input is read every 711 µs. The appropriate ADC

Table 10. 10-BIT ADC OUTPUT CODE VS. VIN

V_{CC} (3.3 V_{IN}) (Note 1)

VCCP

channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Register 0x55, Bits <7:5>	Channel Selected
001	V _{CCP}
010	V _{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Table 9. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description	
<4>	1: Averaging Off	
<5>	1: Bypass Input Attenuators	
<6>	1: Single-channel Convert Mode	

TACH1 Minimum High Byte (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

ADC Output

Temperature Measurement Method

Local Temperature Measurement

The ADT7475 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 11 and Table 12.

Theoretically, the temperature sensor and ADC can measure temperatures from 128° C to $+127^{\circ}$ C (or 64° C to $+191^{\circ}$ C in the extended temperature range) with a resolution of 0.25° C.

However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7475 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7475 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about -2 mV/

Nulling Out Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D- traces around a

When Bit 7 of Configuration Register 6 (0x10) is set, the default round-robin cycle time increases to 240 ms.

Table 18. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature 1	39
Remote Temperature 2	39
Local Temperature	12

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7475 into single-channel ADC conversion mode. In this mode, the ADT7475 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 19. PROGRAMMING SINGLE-CHANNEL ADCMODE FOR TEMPERATURES

Register 0x55, Bits <7:5>	0x55, Bits <7:5> Channel Selected	
101	Remote 1 Temperature	
110	Local Temperature	
111	Remote 2 Temperature	

Configuration Register 2 (0x73)

Bit <4> = 1, Averaging off Bit <6> = 1, Single-channel Convert Mode

TACH1 Minimum High Byte Register (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the THERM temperature limit registers. When a temperature exceeds its THERM temperature limit, all PWM outputs run at the maximum PWM duty cycle (Register 0x38, Register 0x39, and Register 0x3A). This effectively runs the fans at the fastest allowed speed.

The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting the boost bit in Configuration Register 3 (0x78),

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Table 23. FAN LIMIT REGISTERS

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7475 can be enabled for monitoring. The ADT7475 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently, depending on whether the measured value is being compared to a high or low limit.

High Limit > Comparison Performed Low Limit ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and

Table 24. INTERRUPT STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	1 denotes that a bit in Status Register 2 is set and that Interrupt Status Register 2 should be read.
6	R2T	1 indicates that the Remote 2 Temperature High or Low Limit has been exceeded.
5	LT	

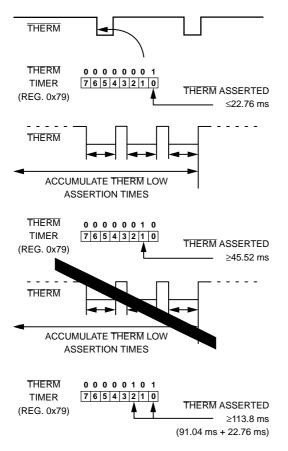


Figure 27. Understanding the THERM Timer

When using the $\overline{\text{THERM}}$ timer, be aware of the following. After a $\overline{\text{THERM}}$ timer read (Register 0x79), the following happens:

- 1. The contents of the timer are cleared on read.
- 2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the THERM timer limit has been exceeded).

If the THERM timer is read during a THERM assertion, the following happens:

- 1. The contents of the timer are cleared.
- 2. Bit 0 of the THERM timer is set to 1 (because a THERM assertion is occurring).
- 3. The THERM timer increments from zero.
- 4. If the THERM timer limit (Register 0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from A THERM Timer Events

The ADT7475 can generate <u>SMBALERTs</u> when a programmable <u>THERM</u> timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions, while capturing longer <u>THERM</u> timer events. Register 0x7A is the <u>THERM</u> timer limit register. This 8-bit register allows a limit from 0 seconds (first <u>THERM</u> assertion) to 5.825 seconds to be set before an <u>SMBALERT</u> is generated. The <u>THERM</u> timer value is compared with the contents of the <u>THERM</u> timer limit register.

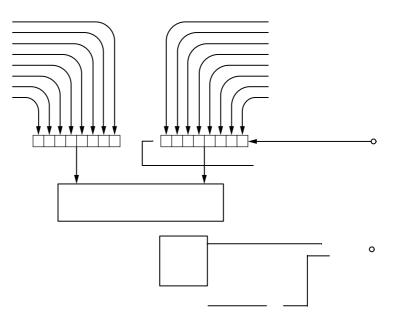


Figure 28. Functional Diagram of the ADT7475 THERM Monitoring Circuitry

If the THERM timer value exceeds the THERM timer limit value, then the F4P bit (Bit 5) of Interrupt Status Register 2 is set, and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Interrupt Mask Register 2 (0x75) masks out SMBALERTs if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 is still set if the THERM timer limit is exceeded.

Figure 28 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (0x7A) causes SMBALERT to be generated on the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms. Enabling and Disabling THERM

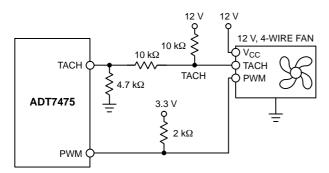


Figure 32. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7475 has four TACH inputs available for fan speed measurement but only three PWM drive outputs. If a fourth

speed control mode or acoustic enhancement mode. See the Programming the Automatic Fan Speed Control Loop section for details.

Operating from 3.3 V Standby

The ADT7475 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring THERM, the THERM timer should be disabled during these states.

Standby Mode

The ADT7475 has been specifically designed to respond to the STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring THERM, the THERM timer should be disabled during these states.

When the V_{CCP}

Step 1: Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

- 1. What ADT7475 functionality will be used?
- PWM2 or <u>SMBALERT</u>?
- TACH4 fan speed measurement or overtemperature THERM function?

The ADT7475 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.

2. How many fans will be supported in the system, three or four?

This influences the choice of whether to use the TACH4 pin or to reconfigure it for the THERM function.

3. Is the CPU fan to be controlled using the ADT7475 or will it run at full speed 100% of the time?

If run at 100%, this frees up a PWM output, but the system is louder.

4. Where will the ADT7475 be physically located in the system?

This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7475 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

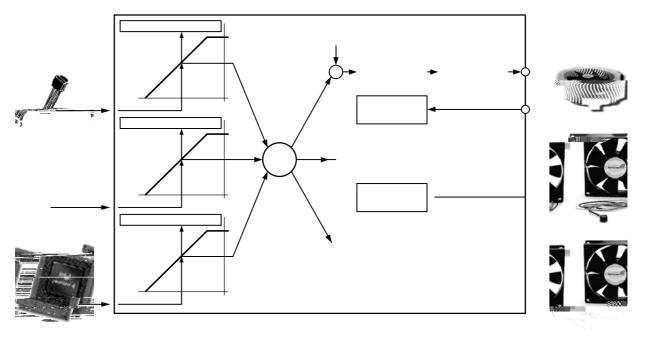


Figure 43. Hardware Configuration Example

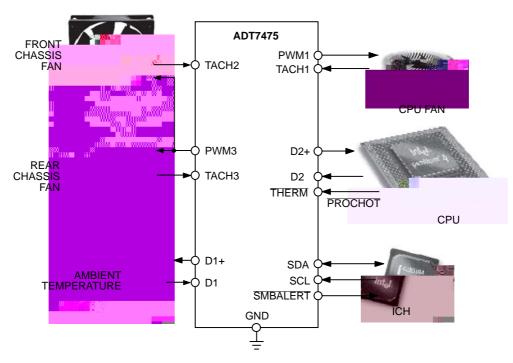


Figure 44. Recommended Implementation 1

Recommended Implementation 2

Configuring the ADT7475 as in Figure 45 provides the system designer with the following features:

- Three PWM outputs for fan control of up to three fan (All three fans can be individually controlled).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- •

Step 2: Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels but the behavior of the fans is also configurable. For example, fans • PWM3 (rear chassis fan) is controlled by the Remote 1 Temperature (ambient).

Example Mux Settings

Bits <7:5> (BHVR), PWM1 Configuration Register (0x5C)

- 101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1
- Bits <7:5> (BHVR), PWM2 Configuration Register (0x5D) 000 = Remote 1 temperature controls PWM2

Bits <7:5> (BHVR), PWM3 Configuration Register (0x5E) 000 = Remote 1 temperature controls PWM3

These settings configure the mux, as shown in Figure 47.

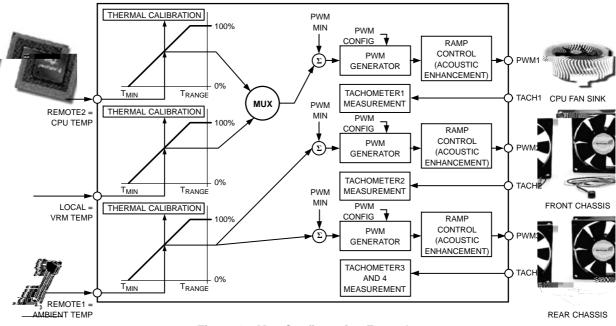


Figure 47. Mux Configuration Example

Step 3: T_{MIN} Settings for Thermal Calibration Channels

 T_{MIN} is the temperature at which the fans turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later in the process. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

 T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: Remote 1, local, and Remote 2 temperatures. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below T_{MIN} T_{HYST} .

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout Section for more details. In some cases, primarily for psycho-acoustic reasons, it is desirable that the fan never switch off below T_{MIN} . Bits <7:5> of Enhanced Acoustics Register 1 (0x62), when set, keep the fans running at the PWM minimum duty cycle, if the temperature should fall below T_{MIN} .

Table 40. T_{MIN} REGISTERS

Register	Description	Default
0x67	Remote 1 Temperature T _{MIN}	0x5A (90°C)
0x68	Local Temperature T _{MIN}	0x5A (90°C)
0x69	Remote 2 Temperature T _{MIN}	0x5A (90°C)

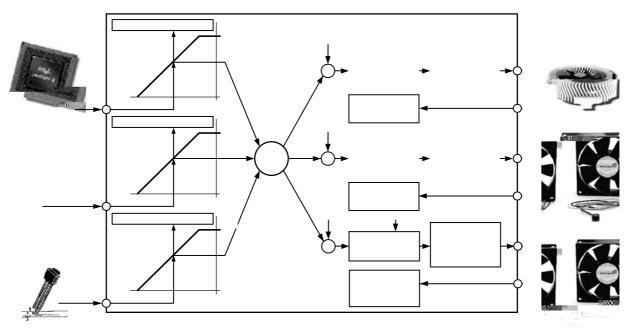
Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below T_{MIN} T_{HYST}.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below T_{MIN} T_{HYST} off (0% PWM duty cycle) when temperature is below T





40% duty cycle. Note that both fans turn on at exactly the

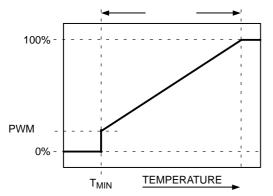


Figure 52. T_{RANGE} Parameter Affects Cooling Slope

temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note that the control range for 4-wire fans is much wider than that for 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20% or less. In extreme cases, some 3-wire fans do not run unless a PWM drive of 60% or more is applied.

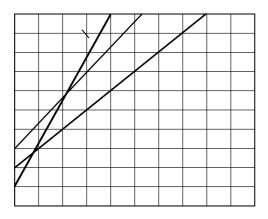
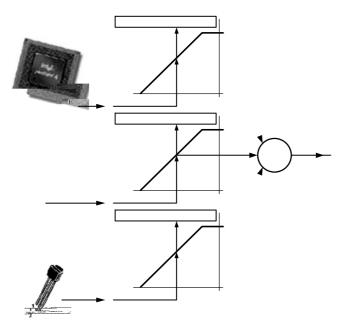




Figure 58. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels







1

Figure 59. How T_{THERM} Relates to Automatic Fan Control

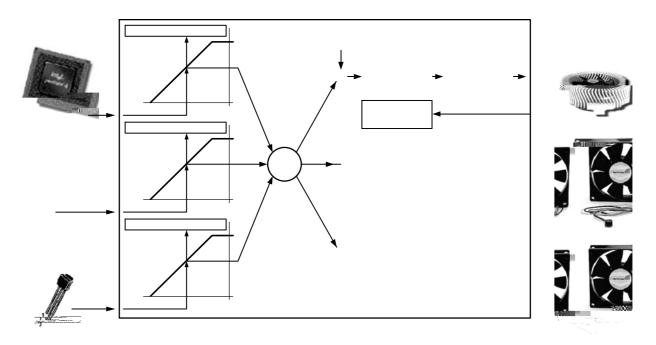


Figure 60. The $T_{\mbox{HYST}}$ Value Applies to Fan On/Off Hysteresis and $\overline{\mbox{THERM}}$ Hysteresis

Enhanced Acoustics Register 1 (0x62)

Bits <2:0> (ACOU1), select the ramp rate for PWM outputs

Table 45. ADT7475 REGISTERS (continued)

Addr

Table 45. ADT7475 REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	Lock- able
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x67	R/W	Remote 1 Temp T _{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x68	R/W	Local Temp T _{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x69	R/W	Remote 2 Temp T _{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x6A	R/W	Remote 1 THERM Temp Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6B	R/W	Local THERM Temp Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6C	R/W	Remote 2 THERM Temp Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6D	R/W	Remote 1 and Local Temp/T _{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	Yes

Table 46. REGISTER 0X10 – CONFIGURATION REGISTER 6 (POWER-ON DEFAULT = 0X00) (Notes 1 and 2)

Bit No.	Mnemonic	R/W	Description
<0>	SLOW Remote 1	R/W	When this bit is set, Fan 1 smoothing times are multiplied x4 for Remote 1 temperature channel (as defined in Register 0x62).
<1>	SLOW Local	R/W	When this bit is set, Fan 2 smoothing times are multiplied x4 for local temperature channel (as defined in Register 0x63).
<2>	SLOW Remote 2	R/W	When this bit is set, Fan 3 smoothing times are multiplied x4 for Remote 2 temperature channel (as defined in Register 0x63).
<3>	THERM in Manual	R/W	When this bit is set, THERM is enabled in manual mode. (Note 1)
<5:4>	Reserved	N/A	Reserved. Do not write to these bits.
<6>	V _{CCP} Low	R/W	$V_{CCP}LO$ = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP}

Register Address	R/W	Description
0x28	Read-only	TACH1 Low Byte
0x29	Read-only	TACH1 High Byte
0x2A	Read-only	TACH2 Low Byte
0x2B	Read-only	TACH2 High Byte
0x2C	Read-only	

Table 50. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Table 53. REGISTER 0X40 - CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0X04)

Bit No.	Mnemonic	R/W	Description
<0>	STRT (Notes 1, 2)	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default powerup limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK) has been set.
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADT7475 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. This bit is lockable.
<2>	RDY	Read-only	This bit is set to 1 by the ADT7475 to indicate only that the device is fully powered up and ready to begin system monitoring.
<3>	FSPD	R/W	When set to 1, this bit runs all fans at max speed as programmed in the PWM current duty cycle registers (0x30 to 0x32). Power-on default = 0. This bit is not locked at any time.
<4>	Vx1	R/W	BIOS should set this bit to a 1 when the ADT7475 is configured to measure current from the controller and to measure the CPU's core voltage. This bit allows monitoring software to display CPU watts usage. This bit is lockable.
<5>	FSPDIS	R/W	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
<6>	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. This allows the ADT7475 to be used with SMBus controllers that cannot handle SMBus timeouts. This bit is lockable.
<7>	RES		Reserved.

Bit 0 (STRT) of Configuration Register 1 (0x40) remains writable after the lock bit is set.
 When monitoring is disabled, PWM outputs always go to 100% for thermal protection.

Table 54. REGISTER 0X41 – INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	
<1>	V _{CCP}	Read-only	V

Table 55. REGISTER 0X42 - INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
<1>	OVT	Read-only	OVT = 1 indicates that one of the THERM overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below THERM – T _{HYST} .
<2>	FAN1	Read-only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
<3>	FAN2	Read-only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM2 output is off.
<4>	FAN3	Read-only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
<5>	F4P	Read-only	F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
		R/W	When Pin 9 is programmed as a GPIO output, writing to this bit determines the logic output of the GPIO.
		Read-only	If Pin 9 is configured as the THERM timer input for THERM monitoring, this bit is set when the THERM assertion time exceeds the limit programmed in the THERM timer limit register (0x7A).
<6>	D1	Read-only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read-only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 56. VOLTAGE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x46	R/W	V _{CCP} Low Limit	0x00
0x47	R/W	V _{CCP} High Limit	0xFF
0x48	R/W	V _{CC} Low Limit	0x00
0x49	R/W	V _{CC} High Limit	0xFF

 Setting the Configuration Register 1 Lock bit has no effect on these registers.
 High limits: an interrupt is generated when a value exceeds its high limit (> comparison); low limits: an interrupt is generated when a value is equal to or below its low limit (\leq comparison).

Table 57. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x4E	R/W	Remote 1 Temperature Low Limit	0x81
0x4F	R/W	Remote 1 Temperature High Limit	0x7F
0x50	R/W	Local Temperature Low Limit	0x81
0x51	R/W	Local Temperature High Limit	0x7F
0x52	R/W	Remote 2 Temperature Low Limit	0x81
0x53	R/W	Remote 2 Temperature High Limit	0x7F

1. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 Lock bit has no effect on these registers.

2. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); low limits: an interrupt is generated when a value is equal to or below its low limit (\leq comparison).

Register Address	R/W	Description	Power-On Default
0x54	R/W	TACH1 Minimum Low Byte	0xFF
0x55	R/W	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	R/W	TACH2 Minimum Low Byte	0xFF
0x57	R/W	TACH2 Minimum High Byte	0xFF
0x58	R/W	TACH3 Minimum Low Byte	0xFF
0x59	R/W	TACH3 Minimum High Byte	0xFF
0x5A	R/W	TACH4 Minimum Low Byte	0xFF
0x5B	R/W	TACH4 Minimum High Byte	0xFF

Table 58. FAN TACHOMETER LIMIT REGISTERS (Note 1)

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 59. REGISTER 0X55 – TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0XFF)

Bit No.	Mnemonic	R/W	Description
<4:0>	Reserved	Read-only	These bits are reserved when Bit 6 of Configuration Register 2 (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte register.
<7:5>	SCADC	R/W	When Bit 6 of Configuration Register 2 (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC makes measurements. Otherwise, these bits represent Bits <7:5> of the TACH1 minimum high byte register.

Table 60. PWM CONFIGURATION REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x5C	R/W	PWM1 Configuration	0x62
0x5D	R/W	PWM2 Configuration	0x62
0x5E	R/W	PWM3 Configuration	0x62

1. These registers become read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 61. REGISTER 0X05C, REGISTER 0X5D, AND REGISTER 0X5E – PWM CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X62)

Bit No.	Mnemonic	R/W	Description	
<2:0>	SPIN	R/W	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, the TACH measurement reads 0xFFFF and Interrupt Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, the Interrupt Status Register 2 bit is not set, even if the fan has not started. 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 4 sec	
<4>	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output so that 100% duty cycle corresponds to a logic low output.	
<7:5>	BHVR	R/W	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = Local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs full speed. 100 = PWMx disabled (default). 101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = Fastest speed calculated by all three temperature channel controls PWMx. 111 = Manual Mode. PWM duty cycle registers (0x30 to 0x32) become writable.	

Table 62. TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x5F	R/W	Remote 1 T _{RANGE} /PWM1 Frequency	0xC4
0x60	R/W	Local T _{RANGE} /PWM2 Frequency	0xC4
0x61	R/W	Remote 2 T _{RANGE} /PWM3 Frequency	0xC4

1. These registers become read-only when the Configuration Register 1 Lock bit is set. Any subsequent attempts to write to these registers fail.

Table 63. REGISTER 0X05F, REGISTER 0X60, AND REGISTER 0X61 – TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (POWER-ON DEFAULT = 0XC4)

Bit No.	Mnemonic	R/W	Description	
<2:0>	FREQ	R/W	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz	
<3>	HF/LF	R/W	HF/LF = 1, enables high frequency PWM output for 4-wire fans. Once enabled, 3-wire fan specific settings have no effect (this means, pulse stretching).	
<7:4>	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature slope for automatic fan control. $0000 = 2^{\circ}C$ $0001 = 2.5^{\circ}C$ $0010 = 3.33^{\circ}C$ $0011 = 4^{\circ}C$ $0100 = 5^{\circ}C$ $0101 = 6.67^{\circ}C$ $0111 = 10^{\circ}C$ $1000 = 13.33^{\circ}C$ $1001 = 16^{\circ}C$ $1011 = 20^{\circ}C$ $1011 = 26.67^{\circ}C$ $1100 = 32^{\circ}C$ (Default) $1101 = 40^{\circ}C$ $1111 = 80^{\circ}C$	

Table 64. REGISTER 0X62 – ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W	Description
<2:0>	ACOU1	R/W	

Table 65. REGISTER 0X63 - ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit No.	Mnemonic	R/W		Description
<2:0>	ACOU3	R/W	maximum rate of cha the fan speed jumping	t is associated with the local temperature channel, these bits define the nge of the PWMx output for local temperature related changes. Instead of g instantaneously to its newly determined speed, it ramps gracefully at the ese bits. This feature ultimately enhances the acoustics of the fan.
			When Bit 7 of Config	guration Register 6 (0x10) is 0
			Time Slot Increase	Time for 0% to 100%
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	37.5 sec 18.8 sec 12.5 sec 7.5 sec 4.7 sec 3.1 sec 1.6 sec 0.8 sec
			When Bit 7 of Config	guration Register 6 (0x10) is 1
			Time Slot Increase	Time for 0% to 100%
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24	52.2 sec 26.1 sec 17.4 sec 10.4 sec 6.5 sec 4.4 sec 2.2 sec
I			001 = 2	6.5 sec26.1750

Table 67. REGISTER 0X64, REGISTER 0X65, REGISTER 0X66 – PWM MINIMUM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0X80; 50% DUTY CYCLE)

Bit No.	Mnemonic	R/W	Description
<7:0>	PWM Duty Cycle	R/W	These bits define the PWM _{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)

Table 68. T_{MIN} REGISTERS (Note 1 and 2)

Register Address	R/W	Description	Power-On Default
0x67	R/W	Remote 1 Temperature T _{MIN}	0x5A (90°C)
0x68	R/W	Local Temperature T _{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T _{MIN}	0x5A (90°C)

These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
 These registers become read-only when the Configuration Register 1 Lock bit is set. Any subsequent attempts to write to these registers fail.

Table 69. THERM TEMPERATURE LIMIT REGISTERS (Note 1)

Table 71. XNOR TREE TEST ENABLE REGISTER (Note 1)

Register Address	R/W	Bit Name	Description	Power-On Default
0x6F	R/W			

Table 75. REGISTER 0X73

Table 79. REGISTER 0X77 - EXTENDED RESOLUTION REGISTER 2 (Note 1)

Bit No.	Mnemonic	R/W	Description	
<3:2>	TDM1	R/W	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement.	
<5:4>	LTMP	R/W	Local temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement.	
<7:6>	<7:6> TDM2 R/W Remote 2 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement.			
1 If this r	odistor is road	this register a	nd the registers holding the MSB of each reading are frozen until read	

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 80. REGISTER 0X78 - CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 0X00) (Note 1)

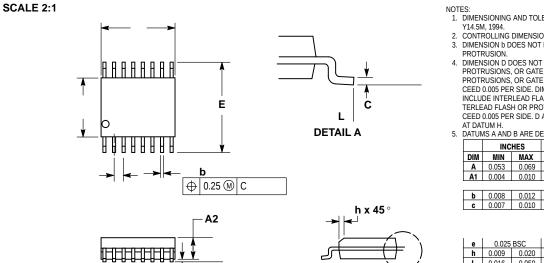
Bit No.	Mnemonic	R/W	Description	
<0>	ALERT Enable	R/W	ALERT = 1, Pin 5 (PWM2/SMBALERT) is configured as an SMBALERT interrupt output to indicate out-of-limit error conditions.	
<1>	THERM	R/W	THERM Enable = 1 enables THERM timer monitoring functionality on Pin 9. Also determined by Bit 0 and Bit 1 (PIN9FUNC) of Configuration Register 4. When THERM is asserted, if the fans are running and the boost bit is set, the fans run at full speed. Alternatively, THERM can be programmed so that a timer is triggered to time how long THERM has been asserted.	
<2>	BOOST	R/W	When THERM is an input and BOOST = 1, assertion of THERM causes all fans to run at the maximum programmed duty cycle for fail-safe cooling.	
<3>	FAST	R/W	FAST = 1, enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4x).	
<4>	DC1			

Table 83. REGISTER 0X7B - TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0X55)

<1:0> FAN1 R/W Sets the number of pulses to be counted when measuring Fan 1 speed. Can be used to	Bit No.	Mnemonic	R/W	Description
$\begin{array}{c} \text{Prive} \\ Pr$	<1:0>	FAN1	R/W	Pulses Counted 00 = 1 01 = 2 (Default) 10 = 3

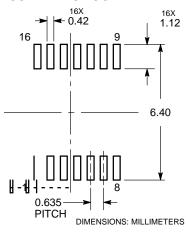


QSOP16 CASE 492-01 ISSUE A



SOLDERING FOOTPRINT

A1



DETÁIL A

- NOTES:
 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EX-CEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERJEAD ELASH OR PROTRUSION. IN INCLUDE INTERLEAD FLASH OR PROTRUSION. IN-TERLEAD FLASH OR PROTRUSION SHALL NOT EX-CEED 0.005 PER SIDE. D AND E1 ARE DETERMINED

AT DATUM H. 5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INC	HES	
DIM	MIN	MAX	
Α	0.053	0.069	
A1	0.004	0.010	
b	0.008	0.012	

е	0.025 BSC		
h	0.009	0.020	
L	0.016	0.050	

1	М	0 °	8°	

XXXXX	= Specific Device Code
YY	= Year
WW	= Work Week
G	= Pb-Free Package

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