The ADT7475 controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7475 can drive a fan using either a

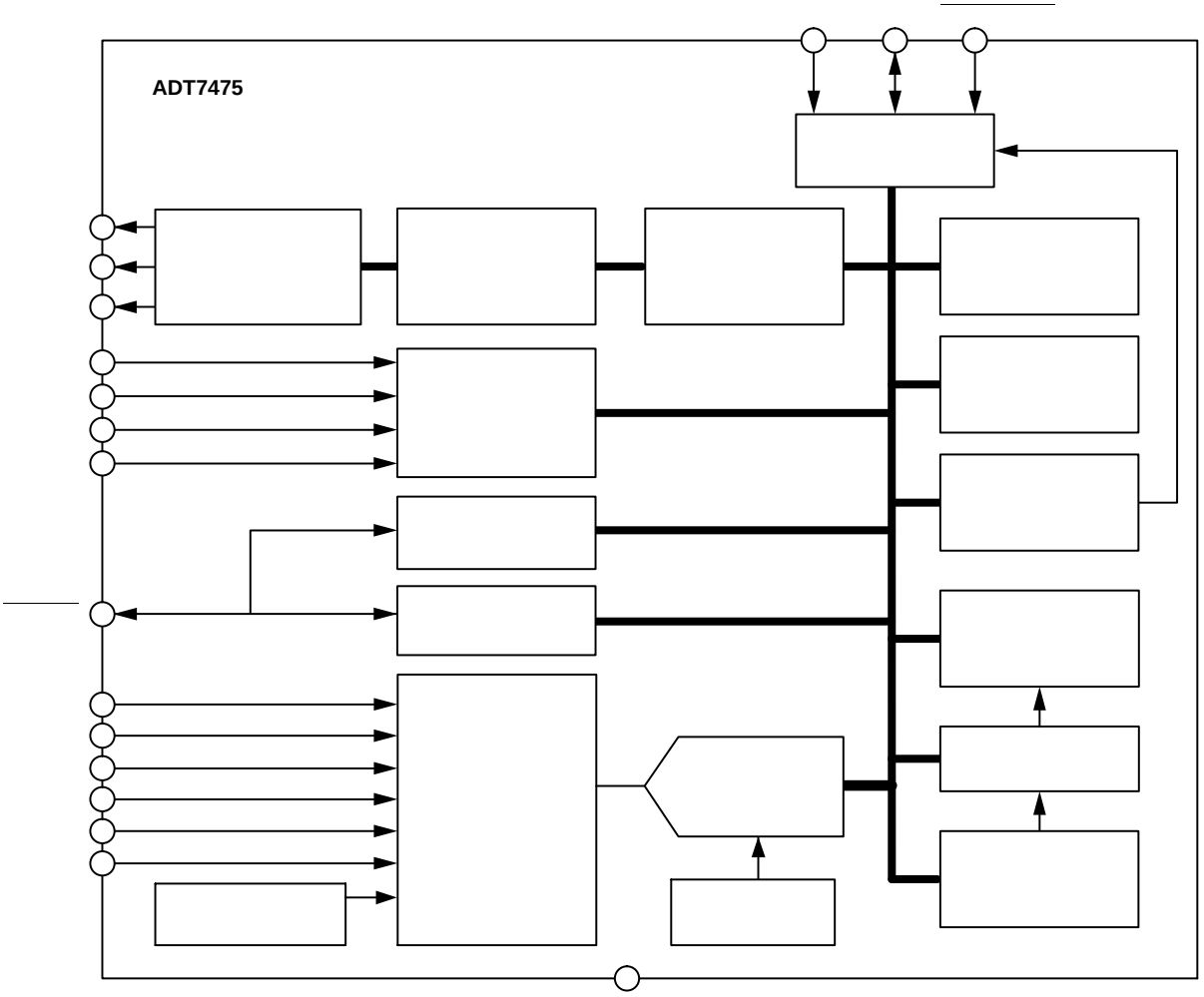


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
	±	
	±	

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
		Ω
		Ω
		Ω
		Ω

Table 4. ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUT CURRENT					
			±		μ
			±		μ
SERIAL BUS TIMING					
					μ
					μ
					μ

TYPICAL PERFORMANCE CHARACTERISTICS

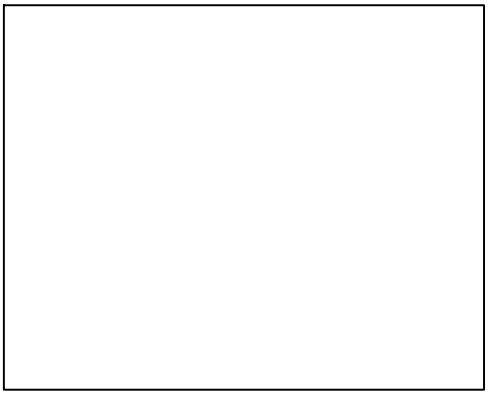


Figure 3. Temperature Error vs. Capacitance Between D+ and D−

Figure 4. Remote Temperature Error vs. PCB Resistance

Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency

Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency

Figure 7. Normal I_{DD} vs. Power Supply

Figure 8. Internal Temperature Error vs. Power Supply Noise

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

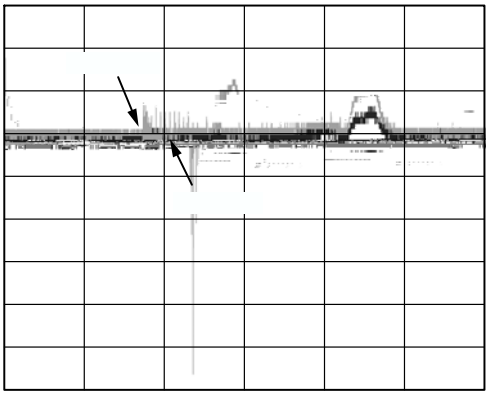


Figure 9. Remote Temperature Error vs. Power Supply Noise Frequency

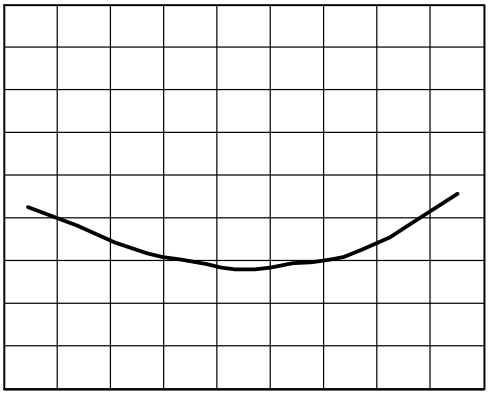


Figure 10. Internal Temperature Error vs. ADT7475 Temperature

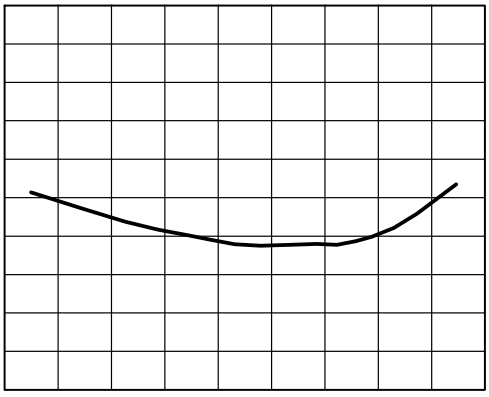


Figure 11. Remote Temperature Error vs. ADT7475 Temperature

Product Description

The ADT7475 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7475 are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Quick Comparison Between ADT7473 and ADT7475

- The ADT7473 supports advanced dynamic T_{MIN} features while the ADT7475 does not.
- Acoustic smoothing is improved on the ADT7475.
- $\overline{\text{THERM}}$ can be selected as an output only on the ADT7475.
- The ADT7475 has two additional configuration registers.
- The ADT7475 has other minor register changes.

The ADT7475 is similar to the ADT7473 in that it is

the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7475, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed, and then data can be written to that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 13. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to write to, which is stored in the address pointer register. The second data byte is the data to write to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7475 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7475 as before, but only the data byte containing the register address is sent, because no data is written to the register see Figure 14.
   A read operation is then performed consisting of the serial bus address; the R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register see Figure 15.
2. If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register see Figure 15.

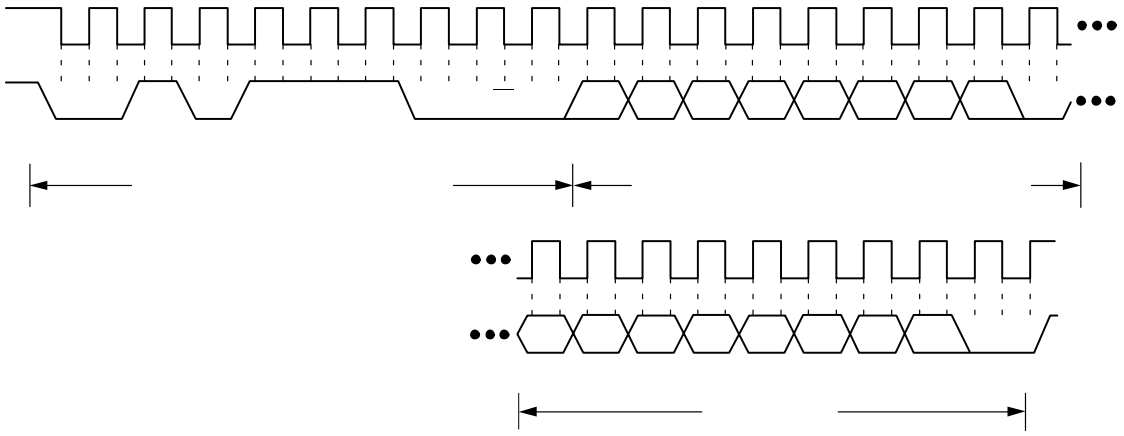


Figure 13. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

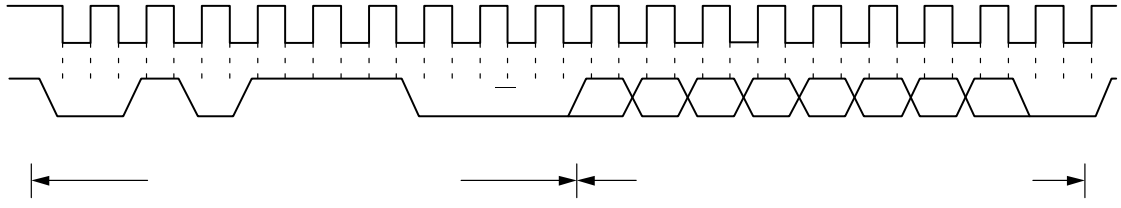


Figure 14. Writing to the Address Pointer Register Only

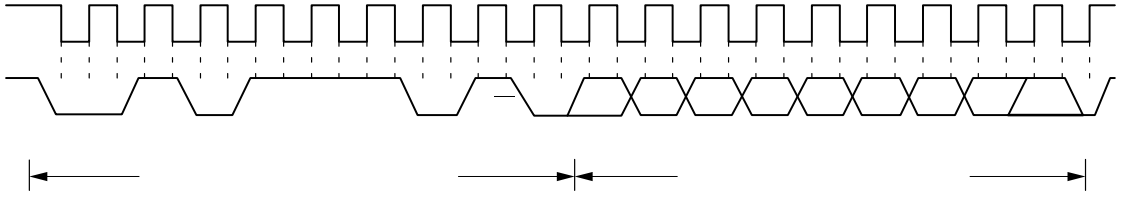


Figure 15. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register if the

master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following events occur:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This general call address must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7475 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus Timeout

The ADT7475 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7475 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Table 5. CONFIGURATION REGISTER 1 (REG. 0X40)

Bit	Description

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7475 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7475 is powered down and powered up again. For more information on which registers are locked, see the Register Tables section.

Voltage Measurement Input

The ADT7475 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings have been made internally, and the results averaged, before being placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This effectively gives a reading 16 times faster (711 μs), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7475 into single-channel ADC conversion mode. In this mode, the ADT7475 can be made to read a single voltage channel only. If the internal ADT7475 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 8. SINGLE-CHANNEL ADC CONVERSION

Register 0x55, Bits <7:5>	Channel Selected

Table 9. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Description

TACH1 Minimum High Byte (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

Table 10. 10-BIT ADC OUTPUT CODE VS. V_{IN}

	ADC Output
V_{CC} (3.3 V_{IN})	V_{CCP}

Temperature Measurement Method

Local Temperature Measurement

The ADT7475 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 11 and Table 12.

Theoretically, the temperature sensor and ADC can measure temperatures from 128°C to +127°C (or 64°C to +191°C in the extended temperature range) with a resolution of 0.25°C.

However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7475 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7475 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/

Nulling Out Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D– traces around a

When Bit 7 of Configuration Register 6 (0x10) is set, the default round-robin cycle time increases to 240 ms.

Table 18. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time (ms)

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7475 into single-channel ADC conversion mode. In this mode, the ADT7475 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 19. PROGRAMMING SINGLE-CHANNEL ADC MODE FOR TEMPERATURES

Register 0x55, Bits <7:5>	Channel Selected

Configuration Register 2 (0x73)

Bit <4> = 1, Averaging off

Bit <6> = 1, Single-channel Convert Mode

TACH1 Minimum High Byte Register (0x55)

Bits <7:5> select the ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ temperature limit registers. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at the maximum PWM duty cycle (Register 0x38, Register 0x39, and Register 0x3A). This effectively runs the fans at the fastest allowed speed.

The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting the boost bit in Configuration Register 3 (0x78),

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Table 23. FAN LIMIT REGISTERS

Register	Description	Default

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7475 can be enabled for monitoring. The ADT7475 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently, depending on whether the measured value is being compared to a high or low limit.

High Limit > Comparison Performed
Low Limit ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and

Table 24. INTERRUPT STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description

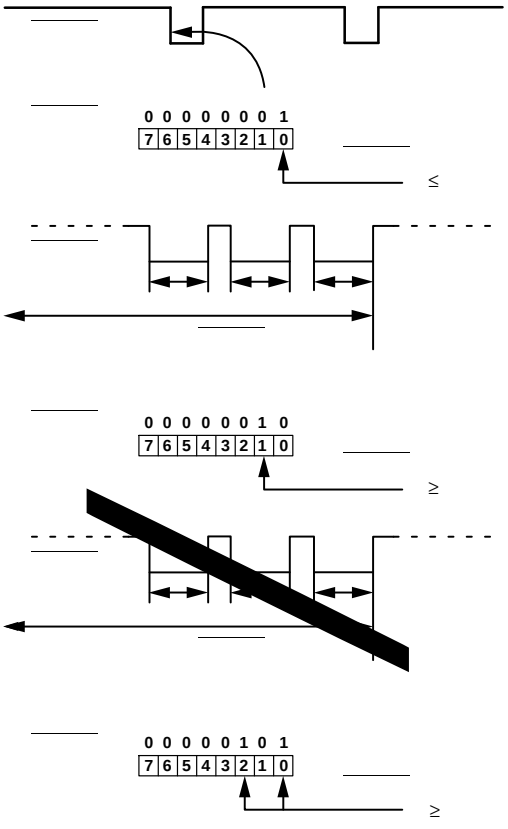


Figure 27. Understanding the $\overline{\text{THERM}}$ Timer

When using the $\overline{\text{THERM}}$ timer, be aware of the following. After a $\overline{\text{THERM}}$ timer read (Register 0x79), the following happens:

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded).

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, the following happens:

1. The contents of the timer are cleared.
2. Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1 (because a $\overline{\text{THERM}}$ assertion is occurring).
3. The $\overline{\text{THERM}}$ timer increments from zero.
4. If the $\overline{\text{THERM}}$ timer limit (Register 0x7A) = 0x00, the F4P bit is set.

Generating $\overline{\text{SMBALERT}}$ Interrupts from A $\overline{\text{THERM}}$ Timer Events

The ADT7475 can generate $\overline{\text{SMBALERT}}$s when a programmable $\overline{\text{THERM}}$ timer limit has been exceeded. This allows the system designer to ignore brief, infrequent $\overline{\text{THERM}}$ assertions, while capturing longer $\overline{\text{THERM}}$ timer events. Register 0x7A is the $\overline{\text{THERM}}$ timer limit register. This 8-bit register allows a limit from 0 seconds (first $\overline{\text{THERM}}$ assertion) to 5.825 seconds to be set before an $\overline{\text{SMBALERT}}$ is generated. The $\overline{\text{THERM}}$ timer value is compared with the contents of the $\overline{\text{THERM}}$ timer limit register.

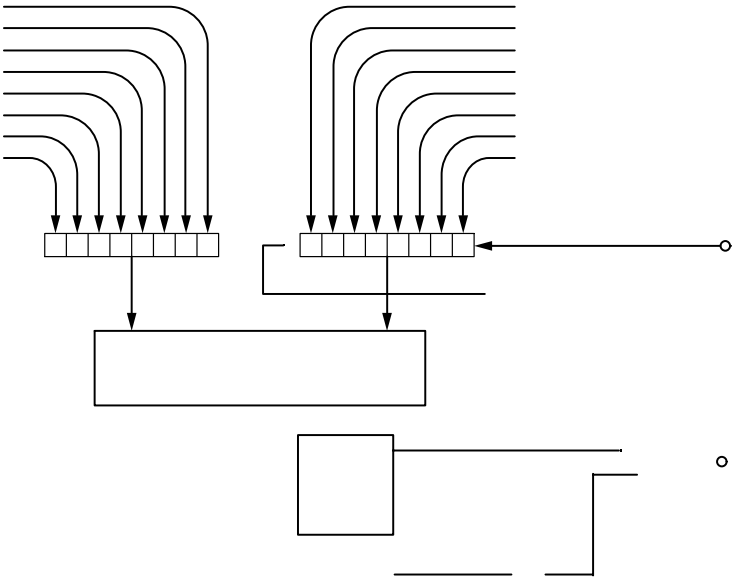


Figure 28. Functional Diagram of the ADT7475 $\overline{\text{THERM}}$ Monitoring Circuitry

If the $\overline{\text{THERM}}$ timer value exceeds the $\overline{\text{THERM}}$ timer limit value, then the F4P bit (Bit 5) of Interrupt Status Register 2 is set, and an $\overline{\text{SMBALERT}}$ is generated. Note that the F4P bit (Bit 5) of Interrupt Mask Register 2 (0x75) masks out $\overline{\text{SMBALERT}}$s if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 is still set if the $\overline{\text{THERM}}$ timer limit is exceeded.

Figure 28 is a functional block diagram of the $\overline{\text{THERM}}$ timer, limit, and associated circuitry. Writing a value of 0x00 to the $\overline{\text{THERM}}$ timer limit register (0x7A) causes $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion. A $\overline{\text{THERM}}$ timer limit value of 0x01 generates an $\overline{\text{SMBALERT}}$ once cumulative $\overline{\text{THERM}}$ assertions exceed 45.52 ms.

Enabling and Disabling $\overline{\text{THERM}}$

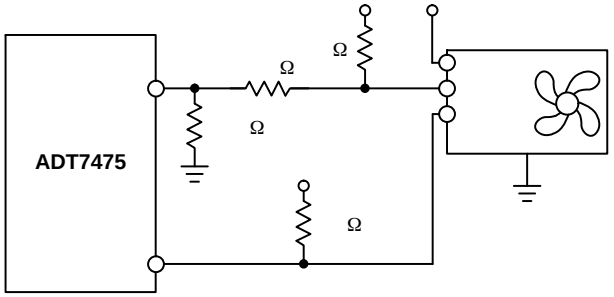


Figure 32. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7475 has four TACH inputs available for fan speed measurement but only three PWM drive outputs. If a fourth

speed control mode or acoustic enhancement mode. See the Programming the Automatic Fan Speed Control Loop section for details.

Operating from 3.3 V Standby

The ADT7475 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

Standby Mode

The ADT7475 has been specifically designed to respond to the STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

When the V_{CCP}

Step 1: Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

1. What ADT7475 functionality will be used?
   - PWM2 or $\overline{\text{SMBALERT}}$?
   - TACH4 fan speed measurement or overtemperature $\overline{\text{THERM}}$ function?

   The ADT7475 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.
2. How many fans will be supported in the system, three or four?

   This influences the choice of whether to use the TACH4 pin or to reconfigure it for the $\overline{\text{THERM}}$ function.
3. Is the CPU fan to be controlled using the ADT7475 or will it run at full speed 100% of the time?

   If run at 100%, this frees up a PWM output, but the system is louder.
4. Where will the ADT7475 be physically located in the system?

   This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7475 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

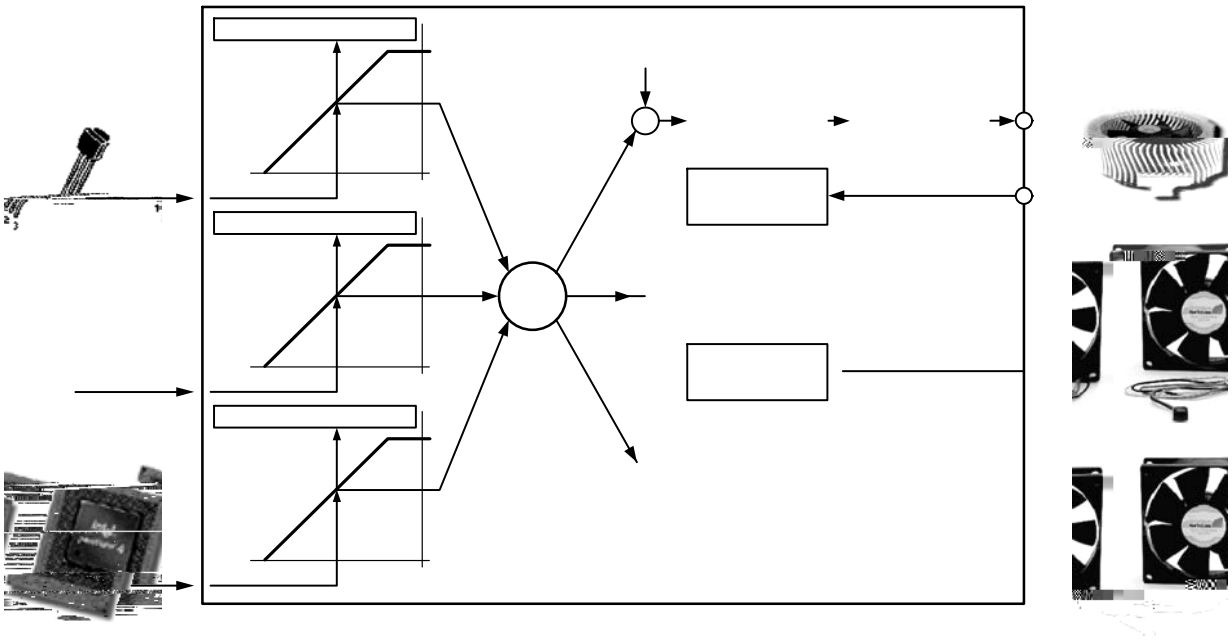


Figure 43. Hardware Configuration Example

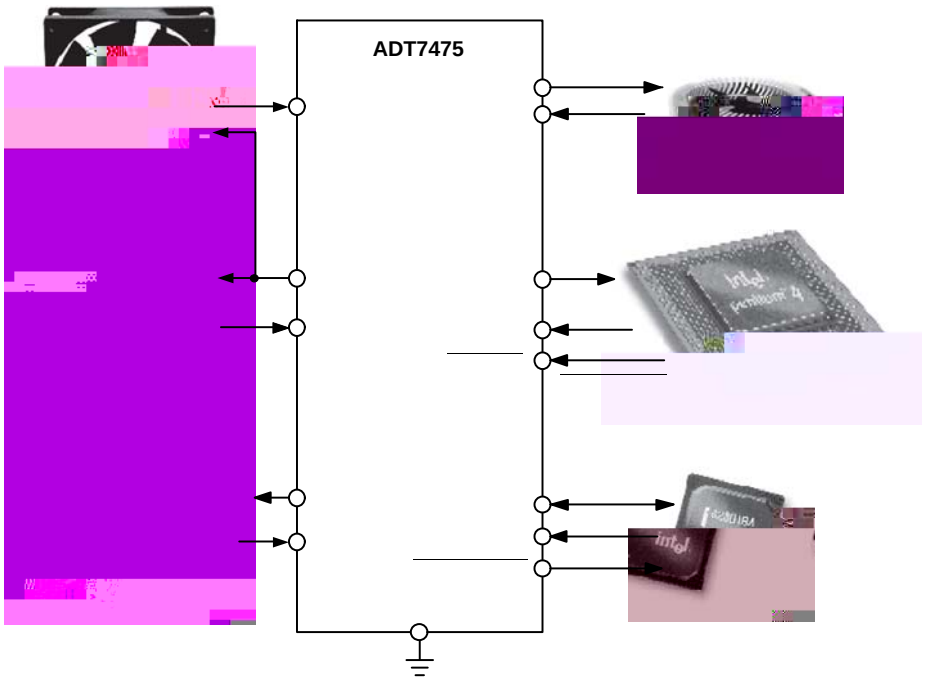


Figure 44. Recommended Implementation 1

Recommended Implementation 2

Configuring the ADT7475 as in Figure 45 provides the system designer with the following features:

- Three PWM outputs for fan control of up to three fan (All three fans can be individually controlled).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
-

Step 2: Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels but the behavior of the fans is also configurable. For example, fans

- PWM3 (rear chassis fan) is controlled by the Remote 1 Temperature (ambient).

Example Mux Settings

Bits <7:5> (BHVR), PWM1 Configuration Register (0x5C)
101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1

Bits <7:5> (BHVR), PWM2 Configuration Register (0x5D)
000 = Remote 1 temperature controls PWM2

Bits <7:5> (BHVR), PWM3 Configuration Register (0x5E)
000 = Remote 1 temperature controls PWM3

These settings configure the mux, as shown in Figure 47.

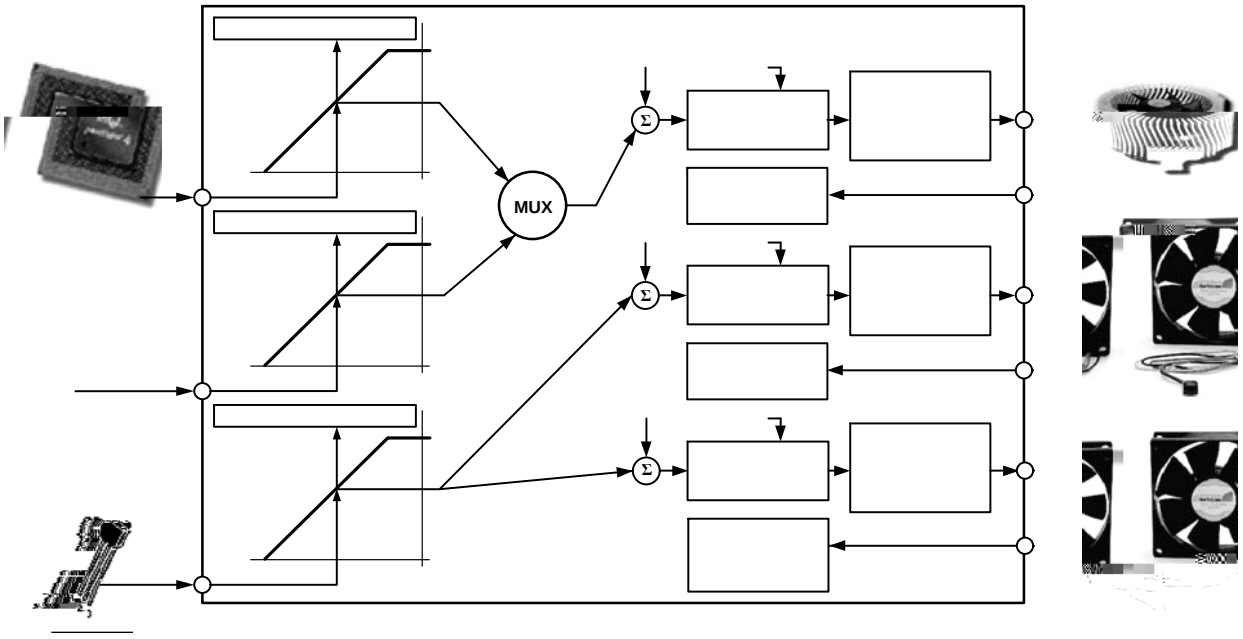


Figure 47. Mux Configuration Example

Step 3: T_{MIN} Settings for Thermal Calibration Channels

T_{MIN} is the temperature at which the fans turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later in the process. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: Remote 1, local, and Remote 2 temperatures. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below T_{MIN} T_{HYST}.

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout Section for more details. In some cases, primarily for psycho-acoustic reasons, it is desirable that the fan never switch off below T_{MIN}. Bits <7:5> of Enhanced Acoustics Register 1 (0x62), when set, keep the fans running at the PWM minimum duty cycle, if the temperature should fall below T_{MIN}.

Table 40. T_{MIN} REGISTERS

Register	Description	Default
		°
		°
		°

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below T_{MIN} T_{HYST}.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below T_{MIN} T_{HYST}.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below T_{MIN} T_{HYST} off (0% PWM duty cycle) when temperature is below T

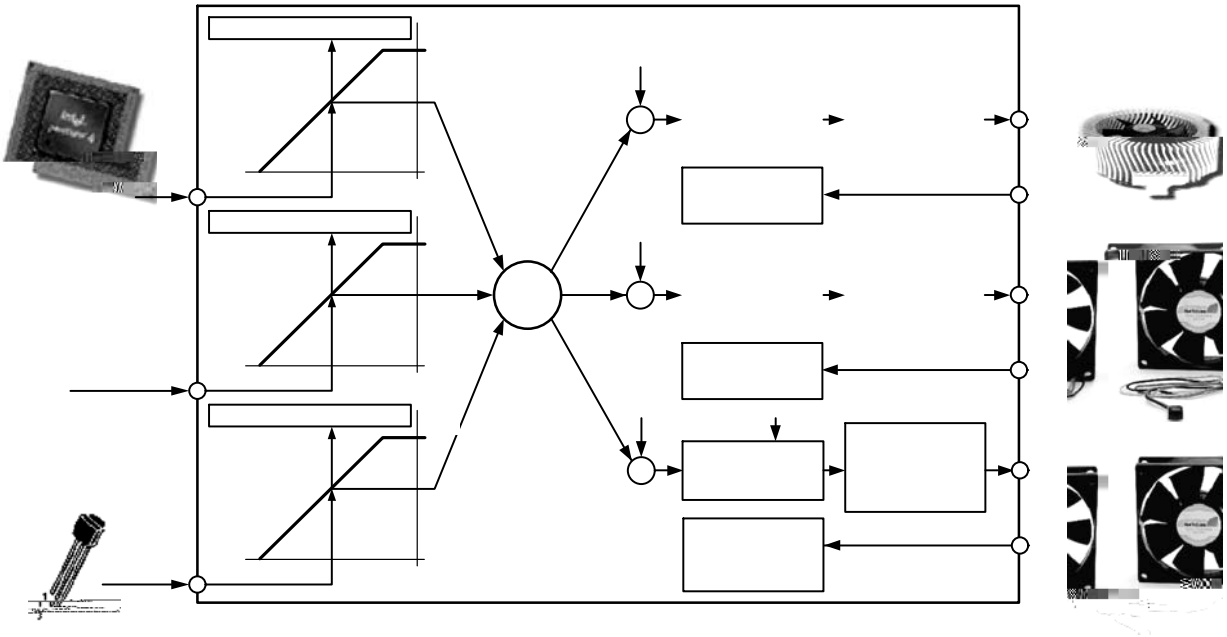


Figure 48. Understanding the T_{MIN} Parameter

40% duty cycle. Note that both fans turn on at exactly the

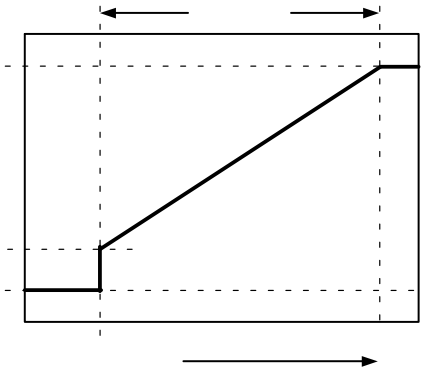


Figure 52. T_{RANGE} Parameter Affects Cooling Slope

temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note that the control range for 4-wire fans is much wider than that for 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20% or less. In extreme cases, some 3-wire fans do not run unless a PWM drive of 60% or more is applied.

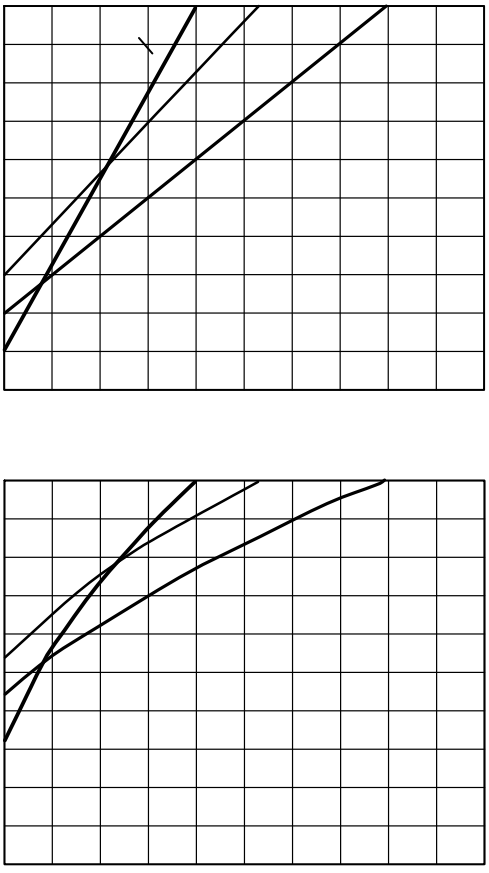


Figure 58. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

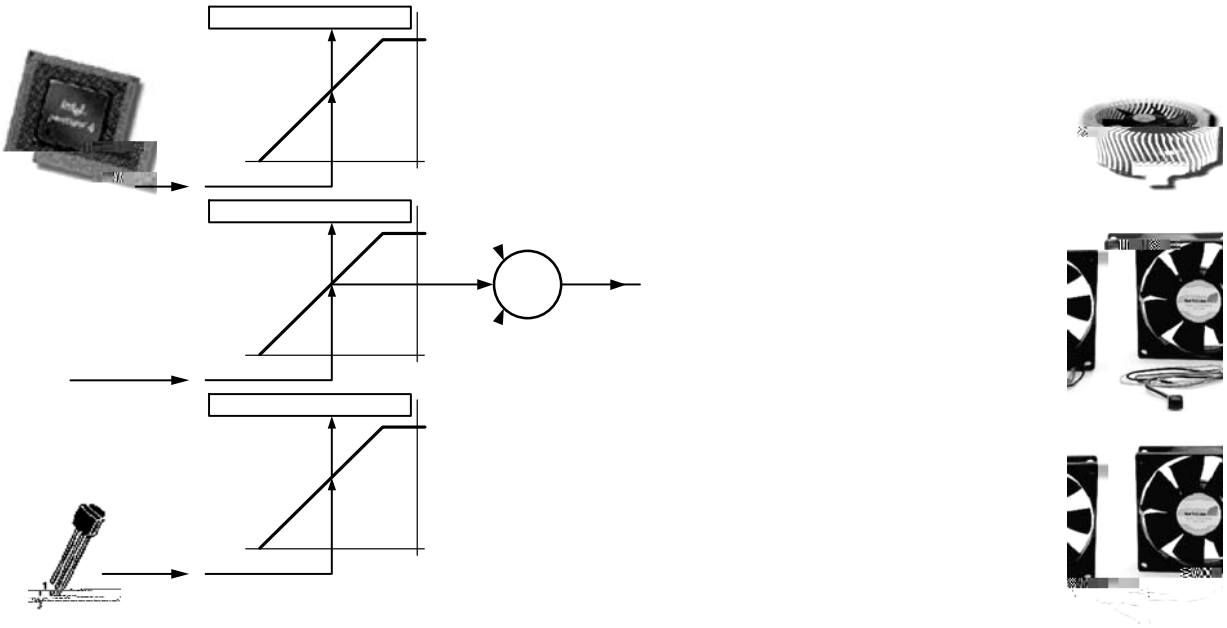


Figure 59. How $T_{\overline{THERM}}$ Relates to Automatic Fan Control

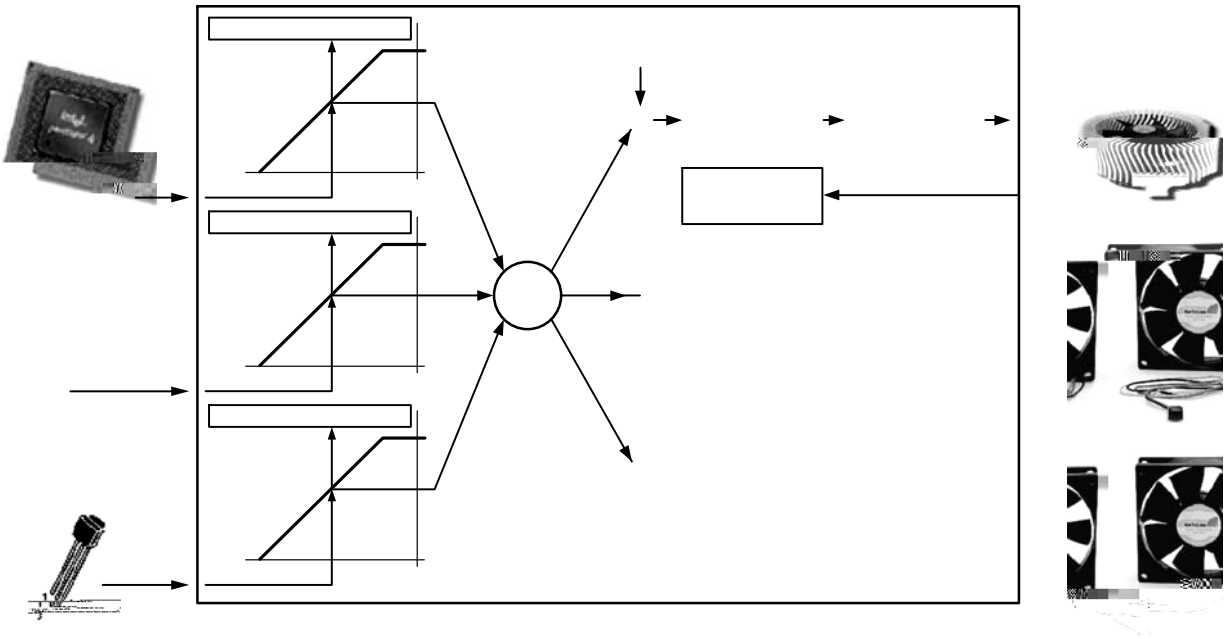


Figure 60. The T_{HYST} Value Applies to Fan On/Off Hysteresis and $\overline{\text{THERM}}$ Hysteresis

Enhanced Acoustics Register 1 (0x62)

Bits <2:0> (ACOU1), select the ramp rate for PWM outputs

Table 45. ADT7475 REGISTERS

Addr		Lock-able

Table 45. ADT7475 REGISTERS

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
		———										
		———										
		———										

Table 46. REGISTER 0X10 − CONFIGURATION REGISTER 6 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

Table 50. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00)

Register Address	R/W	Description

Table 53. REGISTER 0X40 − CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0X04)

Bit No.	Mnemonic	R/W	Description

Table 54. REGISTER 0X41 − INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

Table 55. REGISTER 0X42 − INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

Table 56. VOLTAGE LIMIT REGISTERS

Register Address	R/W	Description	Power-On Default

≤

Table 57. TEMPERATURE LIMIT REGISTERS

Register Address	R/W	Description	Power-On Default

°

≤

Table 58. FAN TACHOMETER LIMIT REGISTERS

Register Address	R/W	Description	Power-On Default

Table 59. REGISTER 0X55 − TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0XFF)

Bit No.	Mnemonic	R/W	Description

Table 60. PWM CONFIGURATION REGISTERS

Register Address	R/W	Description	Power-On Default

Table 61. REGISTER 0X05C, REGISTER 0X5D, AND REGISTER 0X5E − PWM CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X62)

Bit No.	Mnemonic	R/W	Description

Table 62. TEMP T_{RANGE}/PWM FREQUENCY REGISTERS

Register Address	R/W	Description	Power-On Default

Table 63. REGISTER 0X05F, REGISTER 0X60, AND REGISTER 0X61 − TEMP T_{RANGE}/PWM FREQUENCY REGISTERS (POWER-ON DEFAULT = 0XC4)

Bit No.	Mnemonic	R/W	Description

Table 64. REGISTER 0X62 − ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

Table 65. REGISTER 0X63 − ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description
			When Bit 7 of Configuration Register 6 (0x10) is 0 **Time Slot Increase Time for 0% to 100%** **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase Time for 0% to 100%**

Table 67. REGISTER 0X64, REGISTER 0X65, REGISTER 0X66 − PWM MINIMUM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0X80; 50% DUTY CYCLE)

Bit No.	Mnemonic	R/W	Description

Table 68. T_{MIN} REGISTERS

Register Address	R/W	Description	Power-On Default
			◦
			◦
			◦

Table 69. $\overline{\text{THERM}}$ TEMPERATURE LIMIT REGISTERS

Table 71. XNOR TREE TEST ENABLE REGISTER

Register Address	R/W	Bit Name	Description	Power-On Default

Table 75. REGISTER 0X73

Table 79. REGISTER 0X77 − EXTENDED RESOLUTION REGISTER 2

Bit No.	Mnemonic	R/W	Description

Table 80. REGISTER 0X78 − CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 0X00)

Bit No.	Mnemonic	R/W	Description

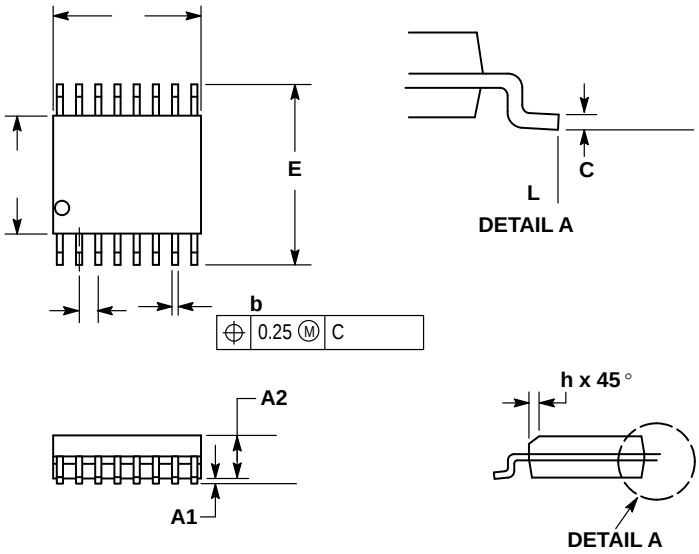
Table 83. REGISTER 0X7B − TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0X55)

Bit No.	Mnemonic	R/W	Description

QSOP16
CASE 492−01
ISSUE A

DATE 23 MAR 2011

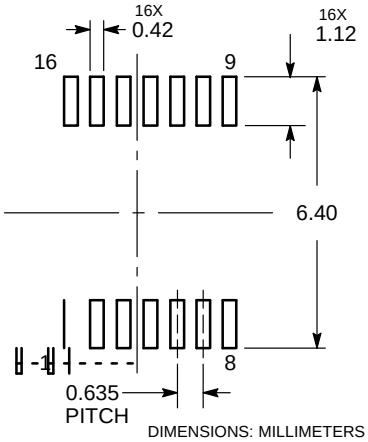
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INCHES	
DIM	**MIN**	**MAX**
A	0.053	0.069
A1	0.004	0.010
b	0.008	0.012
c	0.007	0.010
e	0.025 BSC	
h	0.009	0.020
L	0.016	0.050
M	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

XXXXX = Specific Device Code
YY = Year
WW = Work Week
G = Pb−Free Package